

74HC05-Q100

Hex inverter with open-drain outputs

Rev. 1 — 9 July 2012

Product data sheet

1. General description

The 74HC05-Q100 is a high-speed Si-gate CMOS device that complies with JEDEC standard no. 7A.

The 74HC05-Q100 contains six inverters. The outputs of the 74HC05-Q100 are open-drain and can be connected to other open-drain outputs to implement active-LOW wired-OR or active-HIGH wired-AND functions. The open-drain outputs require pull-up resistors to perform correctly.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - ◆ Specified from -40 °C to $+85\text{ °C}$ and from -40 °C to $+125\text{ °C}$
- Wide operating voltage 2.0 V to 6.0 V
- Input levels:
 - ◆ For 74HC05-Q100: CMOS level
- Latch-up performance exceeds 100 mA per JESD 78 Class II level A
- ESD protection:
 - ◆ MIL-STD-883, method 3015 exceeds 2000 V
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V (C = 200 pf, R = 0 Ω)
- Multiple package options

3. Ordering information

Table 1. Ordering information

| Type number | Package | | | Version |
|---------------|-------------------|----------|--|----------|
| | Temperature range | Name | Description | |
| 74HC05D-Q100 | -40 °C to +125 °C | SO14 | plastic small outline package; 14 leads; body width 3.9 mm | SOT108-1 |
| 74HC05PW-Q100 | -40 °C to +125 °C | TSSOP14 | plastic thin shrink small outline package; 14 leads; body width 4.4 mm | SOT402-1 |
| 74HC05BQ-Q100 | -40 °C to +125 °C | DHVQFN14 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm | SOT762-1 |

4. Functional diagram

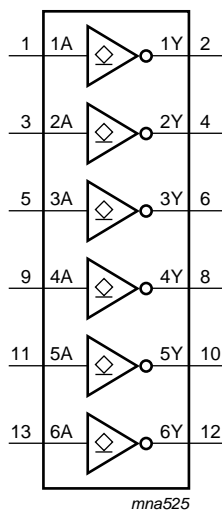


Fig 1. Logic symbol

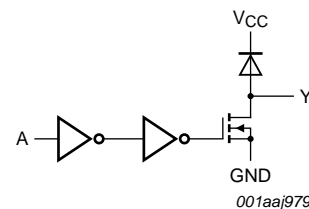


Fig 2. Logic diagram (one gate)

5. Pinning information

5.1 Pinning

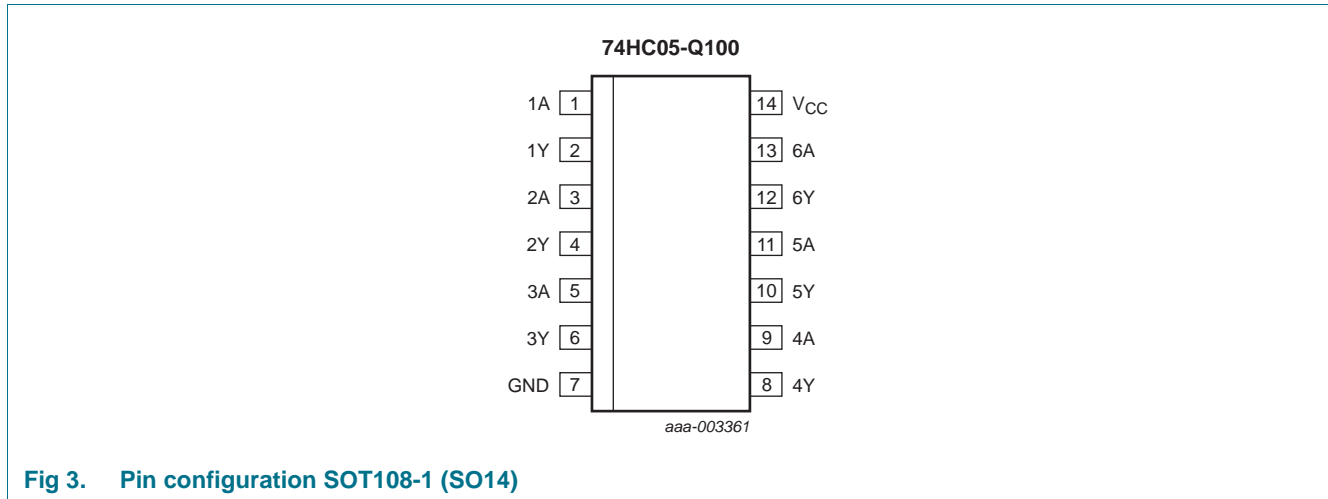


Fig 3. Pin configuration SOT108-1 (SO14)

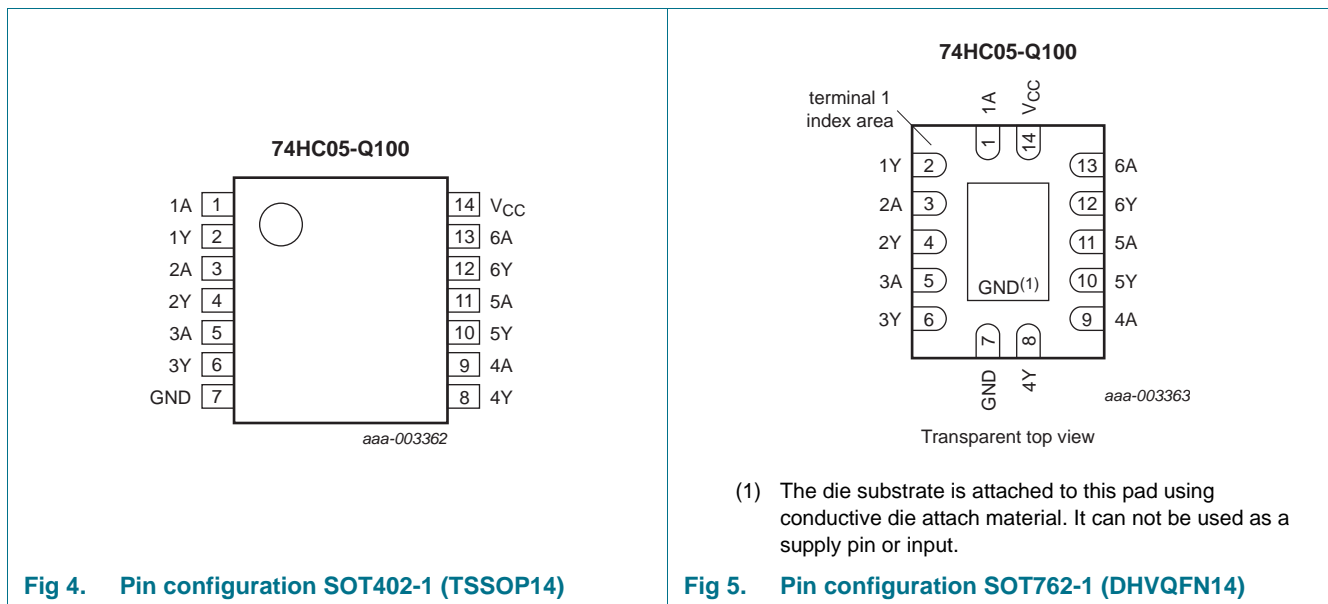


Fig 4. Pin configuration SOT402-1 (TSSOP14)

Fig 5. Pin configuration SOT762-1 (DHVQFN14)

5.2 Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|-----------------|--------------------|----------------|
| 1A to 6A | 1, 3, 5, 9, 11, 13 | data input |
| 1Y to 6Y | 2, 4, 6, 8, 10, 12 | data output |
| GND | 7 | ground (0 V) |
| V _{CC} | 14 | supply voltage |

6. Functional description

Table 3. Function table^[1]

| Input | Output |
|-------|--------|
| nA | nY |
| L | Z |
| H | L |

[1] H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-------------------------|--|----------|-------------------------|------|
| V_{CC} | supply voltage | | -0.5 | +7 | V |
| I_{IK} | input clamping current | $V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$ | [1] - | ± 20 | mA |
| I_{OK} | output clamping current | $V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$ | [1] - | ± 20 | mA |
| V_O | output voltage | | [1] -0.5 | $V_{CC} + 0.5\text{ V}$ | V |
| I_O | output current | $V_O < V_{CC} + 0.5\text{ V}$ | - | 25 | mA |
| I_{CC} | supply current | | - | 50 | mA |
| I_{GND} | ground current | | -50 | - | mA |
| T_{stg} | storage temperature | | -65 | +150 | °C |
| P_{tot} | total power dissipation | | [2] - | 500 | mW |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SO14 package: P_{tot} derates linearly with 8 mW/K above 70 °C.
 For TSSOP14 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.
 For DHVQFN14 packages: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|-------------------------------------|-------------------------|-----|------|----------|------|
| V_{CC} | supply voltage | | 2.0 | 5.0 | 6.0 | V |
| V_I | input voltage | | 0 | - | V_{CC} | V |
| V_O | output voltage | | 0 | - | V_{CC} | V |
| T_{amb} | ambient temperature | | -40 | - | +125 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC} = 2.0\text{ V}$ | - | - | 625 | ns/V |
| | | $V_{CC} = 4.5\text{ V}$ | - | 1.67 | 139 | ns/V |
| | | $V_{CC} = 6.0\text{ V}$ | - | - | 83 | ns/V |

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|-----------------|--|---|-------|------|------|------------------|------|-------------------|------|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 2.0 V | 1.5 | 1.2 | - | 1.5 | - | 1.5 | - | V |
| | | V _{CC} = 4.5 V | 3.15 | 2.4 | - | 3.15 | - | 3.15 | - | V |
| | | V _{CC} = 6.0 V | 4.2 | 3.2 | - | 4.2 | - | 4.2 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 2.0 V | - | 0.8 | 0.5 | - | 0.5 | - | 0.5 | V |
| | | V _{CC} = 4.5 V | - | 2.1 | 1.35 | - | 1.35 | - | 1.35 | V |
| | | V _{CC} = 6.0 V | - | 2.8 | 1.8 | - | 1.8 | - | 1.8 | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | | | |
| | | I _O = 20 μA; V _{CC} = 2.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 20 μA; V _{CC} = 4.5 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 20 μA; V _{CC} = 6.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 4.0 mA; V _{CC} = 4.5 V | - | 0.15 | 0.26 | - | 0.33 | - | 0.4 | V |
| | I _O = 5.2 mA; V _{CC} = 6.0 V | - | 0.16 | 0.26 | - | 0.33 | - | 0.4 | V | |
| I _I | input leakage current | V _I = V _{CC} or GND; V _{CC} = 6.0 V | - | - | ±0.1 | - | ±1 | - | ±1 | μA |
| I _{OZ} | OFF-state output current | per input pin; V _I = V _{IL} ; V _O = V _{CC} or GND; other inputs at V _{CC} or GND; V _{CC} = 6.0 V; I _O = 0 A | - | - | ±0.5 | - | ±5.0 | - | ±10 | μA |
| I _{CC} | supply current | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V | - | - | 2.0 | - | 20 | - | 40 | μA |
| C _I | input capacitance | | - | 3.5 | - | - | - | - | - | pF |

10. Dynamic characteristics

Table 7. Dynamic characteristics

$GND = 0\text{ V}$; for test circuit see [Figure 7](#).

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +125 °C | | Unit |
|------------------|------------------------------------|---|---------------------|-----|-----|-------------------|--------------|------|
| | | | Min | Typ | Max | Max (85 °C) | Max (125 °C) | |
| t _{PLZ} | LOW to OFF-state propagation delay | nA to nY; see Figure 6 | | | | | | |
| | | V _{CC} = 2.0 V | - | 20 | 90 | 115 | 135 | ns |
| | | V _{CC} = 4.5 V | - | 11 | 18 | 23 | 27 | ns |
| | | V _{CC} = 6.0 V | - | 10 | 15 | 20 | 23 | ns |
| t _{PZL} | OFF-state to LOW propagation delay | nA to nY; see Figure 6 | | | | | | |
| | | V _{CC} = 2.0 V | - | 22 | 90 | 115 | 135 | ns |
| | | V _{CC} = 4.5 V | - | 9 | 18 | 23 | 27 | ns |
| | | V _{CC} = 6.0 V | - | 8 | 15 | 20 | 23 | ns |
| t _{THL} | HIGH to LOW output transition time | see Figure 6 | | | | | | |
| | | V _{CC} = 2.0 V | - | 18 | 75 | 95 | 110 | ns |
| | | V _{CC} = 4.5 V | - | 6 | 15 | 19 | 22 | ns |
| | | V _{CC} = 6.0 V | - | 5 | 13 | 16 | 19 | ns |
| C _{PD} | power dissipation capacitance | per inverter; V _I = GND to V _{CC} ; V _{CC} = 5.0 V | [1] | 4 | - | - | - | pF |

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(0.5 \times C_L \times V_O^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

V_O = output voltage in V (output HIGH);

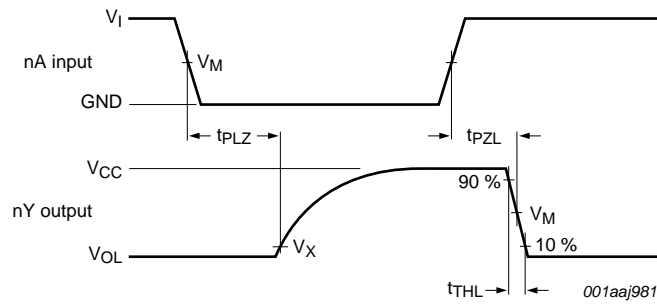
V_{CC} = supply voltage in V;

N = number of inputs switching;

R_L = load resistance in MΩ;

C_L = load capacitance in pF;

11. Waveforms



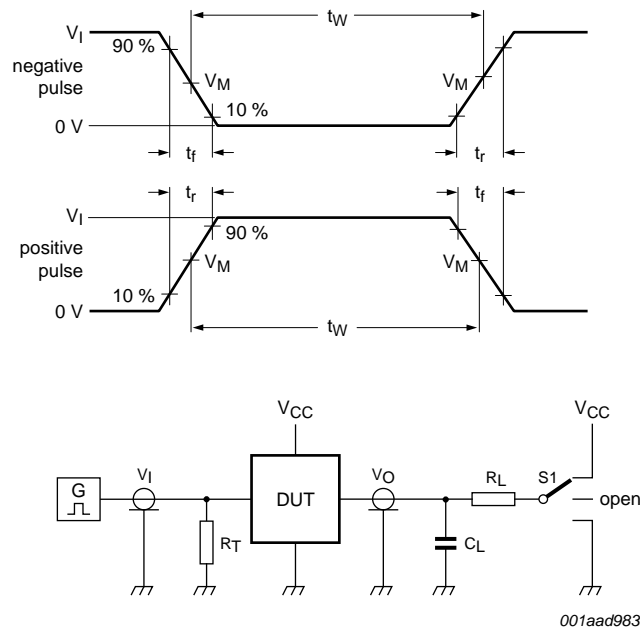
Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 6. The input nA to output nY propagation delays and output transition times

Table 8. Measurement points

| Input | Output | |
|-------------|-------------|-------------|
| V_M | V_M | V_X |
| $0.5V_{CC}$ | $0.5V_{CC}$ | $0.1V_{CC}$ |



Test data is given in [Table 9](#).

Definitions test circuit:

R_T = termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = load capacitance including jig and probe capacitance.

R_L = Load resistance.

Fig 7. Test circuit for measuring switching times

Table 9. Test data

| Input | | Load | | S1 position |
|----------|------------|-------|--------------|--------------------|
| V_I | t_r, t_f | C_L | R_L | t_{pZL}, t_{PLZ} |
| V_{CC} | 6 ns | 50 pF | 1 k Ω | V_{CC} |

12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

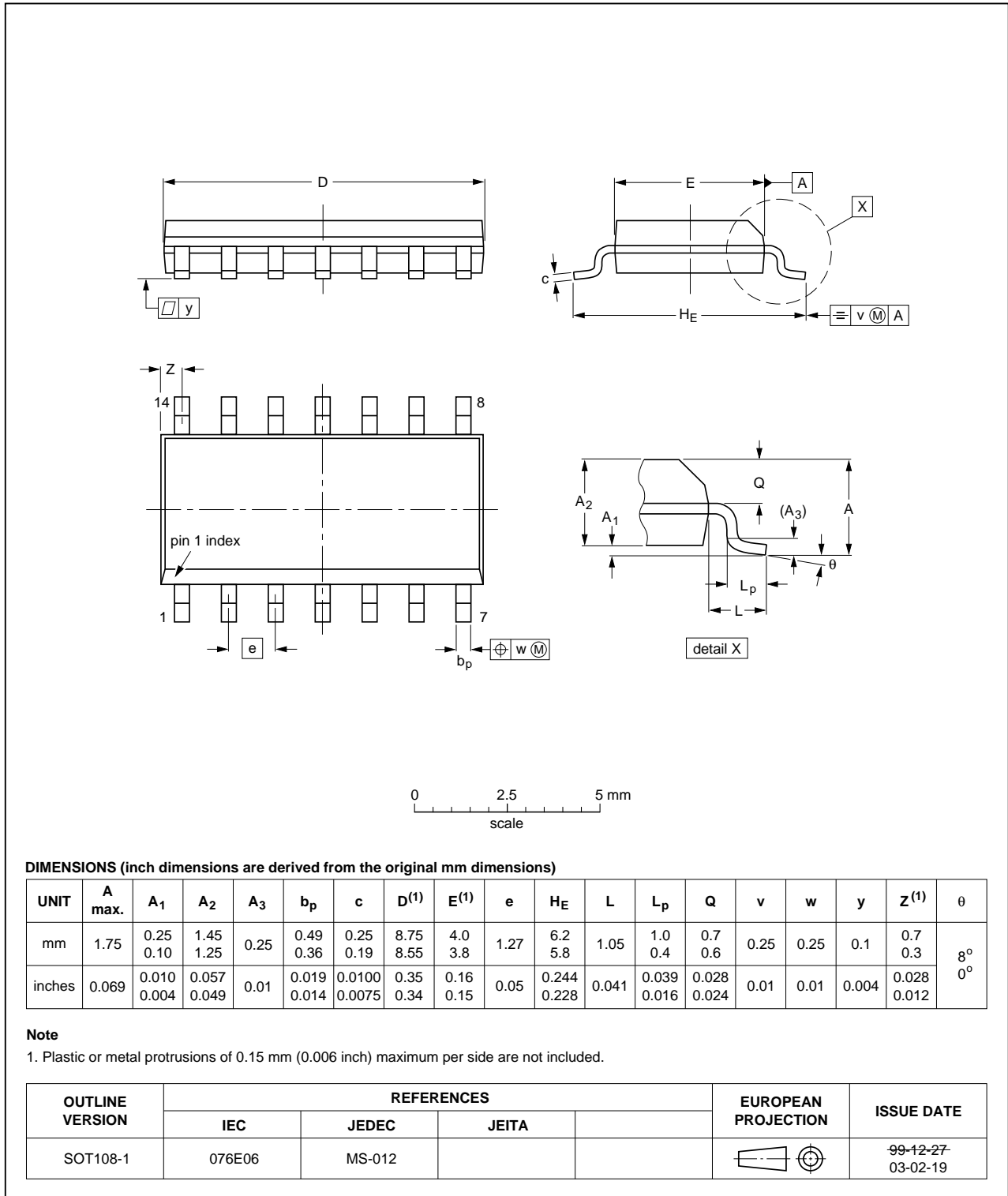


Fig 8. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

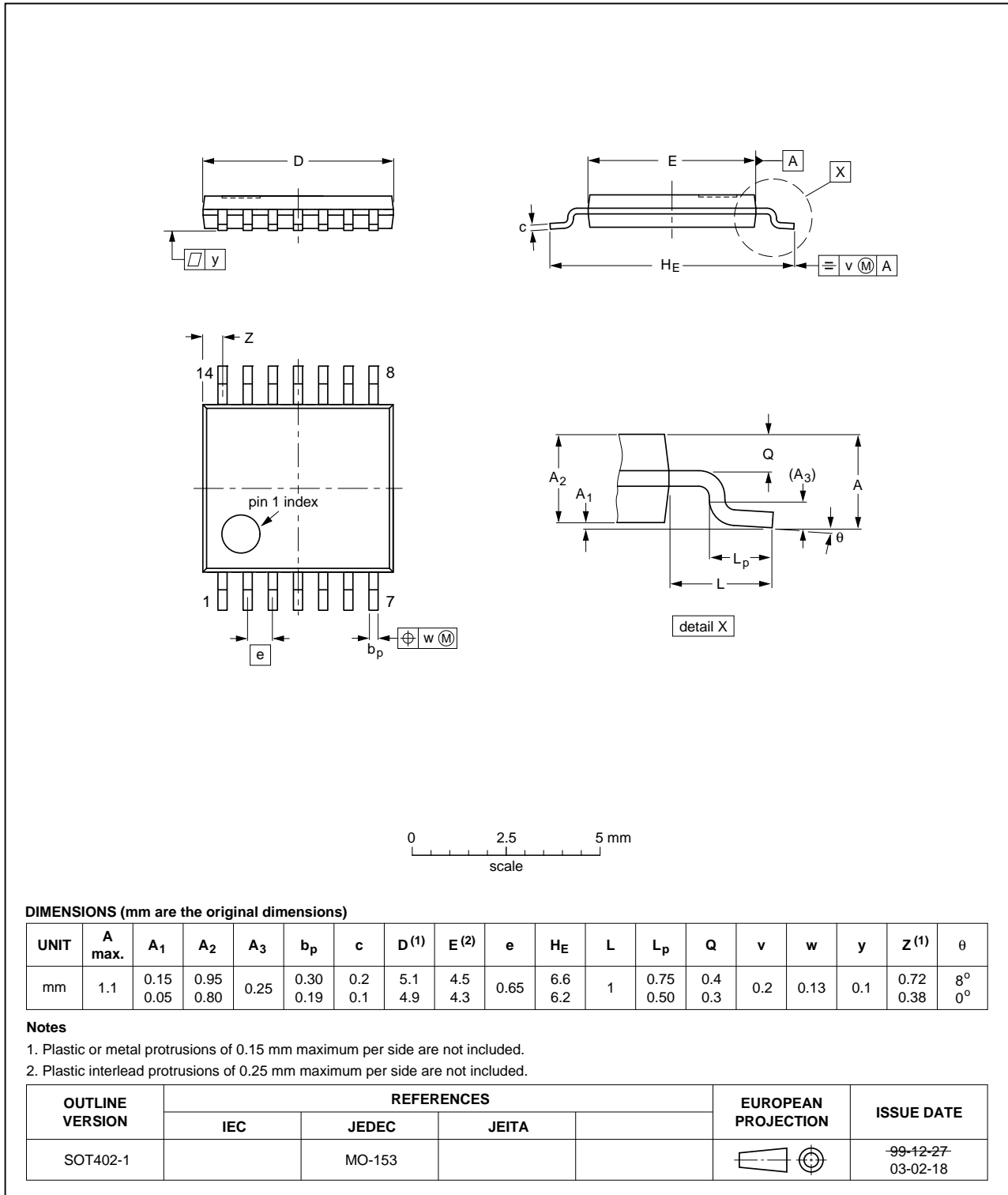


Fig 9. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1

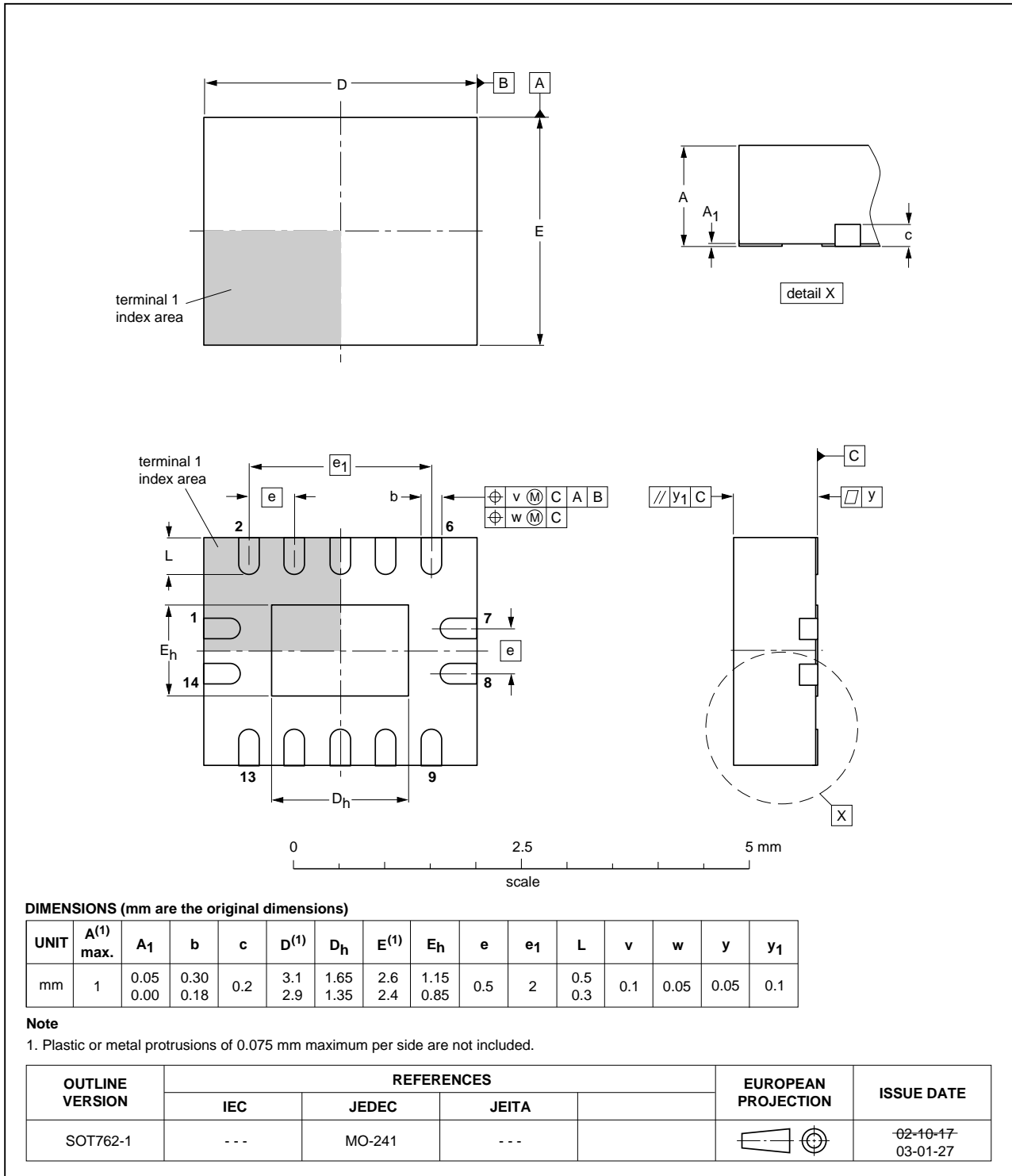


Fig 10. Package outline SOT762-1 (DHVQFN14)

13. Abbreviations

Table 10. Abbreviations

| Acronym | Description |
|---------|---|
| CDM | Charged Device Model |
| CMOS | Complementary Metal-Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |

14. Revision history

Table 11. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---------------|--------------|--------------------|---------------|------------|
| 74HC05_Q100_1 | 20120709 | Product data sheet | - | - |

15. Legal information

15.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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